SYNCHRONIZATION CORRECTION CIRCUIT

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a synchronization

5   correction circuit for correcting synchronization between a

packet transmission cycle and a transfer clock in a receiving

device. The synchronization correction circuit according to

the present invention is applied, for example, to a

Bluetooth-compliant audio data processing circuit.

10   Description of Related Art

A conventional synchronization correction circuit will

hereinafter be described with reference to an example where

such a circuit is applied to a Bluetooth-compliant audio data

processing circuit.

15   "Bluetooth" is one type of specification for data

communications between terminals or other devices. This

specification applies to various types of data communications

conducted between personal computers, printers, mobile

telephones, and the like, principally involving audio data.

20   In a Bluetooth system, communications are conducted

using packets. In other words, for a sound communication

packet, a packet comprising a synchronization word which is

called "sync word" for short, and a payload section is used,

as illustrated in Fig. 14. Here, the sync word is used by the

25   receiver to determine the packet transmission interval.

Furthermore, audio data is contained in the payload section.

There are three types of packets respectively allowing an

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audio data volume of 10 bytes, 20 bytes and 30 bytes, to be stored in the payload section of each packet. Bluetooth specifies respective packet transmission intervals of 1.25 ms, 2.5 ms and 3.75 ms for these types of packets.

In Bluetooth, one of the communication devices, or the like, is set as a master device, the other is taken as a slave device, and bi-directional communications are conducted therebetween by means of time division multiplexing. In other words, the terminal, or the like, set as the master determines the packet transmission interval, and the terminal, or the like, set as the slave is synchronized therewith and communications are conducted therebetween. The master/slave relationship is determined by an appropriate method, for each communication. Fig. 15 is a conceptual diagram for illustrating a Bluetooth communications system. Fig. 15(A) indicates type I, namely, a case where the payload section contains 10 bytes and the packet transmission interval is 1.25 ms; Fig. 15(B) indicates type II, namely, a case where the payload section contains 20 bytes and the packet transmission interval is 2.5 ms; and Fig. 15(C) indicates type III, namely, a case where the payload section contains 30 bytes and the packet transmission interval is 3.75 ms.

Fig. 16 is a block diagram showing the composition of a conventional audio data processing circuit for use with Bluetooth. As shown in Fig. 16, this audio data processing circuit 1600 comprises a baseband processing section 1610 and an audio data converting section 1620. These sections 1610,

1620 are connected respectively via a bus 1630 to a CPU (Central Processing Unit) 1640. During reception, the baseband processing section 1610 extracts the payload sections from the packets and sends same to the audio data

5   converting section 1620, whereas during transmission, it generates packets for transmitting audio data received from the audio data converting section 1620. During reception, the audio data converting section 1620 converts audio data received from the baseband processing section 1610, as

10   necessary, and sends same to the PCM (Pulse Code Modulation) codec interface circuit in a subsequent stage, whereas during transmission, it re-converts audio data received from the PCM codec interface circuit, as necessary, and sends same to the baseband processing section 1610. Bluetooth is compatible

15   with three types of audio data format: CVSD (Continuous Variable Slope Data modulation), A-law and μ-law. On the other hand, the PCM codec interface circuit is compatible with three types of audio data format : Linear, A-law and μ-law.

20   A transfer synchronization signal PCMSYNC and transfer clock PCMCLK are used for sending and receiving data between the audio data converting section 1620 and the PCM codec interface circuit. Fig. 17 illustrates a case where 8-bit/word monoaural data is sampled as 8 kHz. As is

25   understood from the timing chart shown in Fig. 17, the transfer synchronization signal PCMSYNC specifies the transfer cycle for each word, and the transfer clock PCMCLK

specifies the transfer timing for each bit forming the audio data (PCM data). One word may also be composed by 16 bits. In the case of an 8 kHz cycle for the transfer synchronization signal PCMSYNC, the cycle of the transfer clock PCMCLK will

5   be 64 kHz or above (for 8-bit/word) or 128 kHz or above (for 16-bit/word).

Generally, the transfer clock PCMCLK is generated by the system clock of the audio data processing circuit 1600. Furthermore, the transfer synchronization signal PCMSYNC is

10 generated by the transfer clock PCMCLK.

In communications using an audio data processing circuit 1600 of this kind (see Fig. 16), the packet transmission cycle is determined by means of the transfer synchronization signal PCMSYNC from the transmitter circuit (in other words,

15 the circuit generating the packets). Therefore, the transmission period for the PCM data stored in this packet (see Fig. 17) is also determined by synchronization with the transfer synchronization signal PCMSYNC from the transmitter. However, the transfer synchronization signal PCMSYNC used by

20 the receiver terminal is generated within the receiver circuit 1600. In other words, in Fig. 17, whereas the PCM data is generated so as to be synchronized with the system clock of the transmitter-side audio data processing circuit 1600, the transfer synchronization signal PCMSYNC and

25 transfer clock PCMCLK are generated so as to be synchronized with the system clock of the receiver-side audio data processing circuit 1600.

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Here, in cases where the two audio data processing circuits 1600, 1600 conducting communications are running at absolutely the same operating frequency, the PCM data and the transfer synchronization signal PCMSYNC in Fig. 17 will

5   assume completely synchronized states. However, in actual practice, there is often a disparity between the operating frequencies of the receiver-side circuit 1600 and the transmitter-side circuit 1600. If the two circuits 1600, 1600 have different operating frequencies, then the PCM data will

10   not be synchronized completely with the operating clock PCMCLK and the transfer synchronization signal PCMSYNC.

Fig. 18 is a timing chart giving a conceptual illustration of one example of a state where the transfer synchronization signals PCMSYNC of the master and slave do

15   not coincide. In the example in Fig. 18, the frequency of the transfer synchronization signal PCMSYNC generated by the master device is higher than the frequency of the transfer synchronization signal PCMSYNC generated by the slave device. Therefore, on the slave side, the frequency of the received

20   PCM data will be too high compared to the frequency of the transfer synchronization signal PCMSYNC. Consequently, an underflow will be created in the slave device when the received PCM data is transferred from the audio data converting section 1620 to the PCM codec interface circuit.

25   In the master device, on the other hand, the frequency of the received PCM data will be too low compared to the frequency of the transfer synchronization signal PCMSYNC. Therefore, an

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overflow will be created in the master device when the
received PCM data is transferred from the audio data
converting section 1620 to the PCM codec interface circuit.
If an underflow or overflow arises in the transfer of PCM

5   data from the audio data converting section 1620 to the PCM
codec interface circuit, then as a consequence, the
communication quality will decline.

SUMMARY OF THE INVENTION

An object of the present invention is to provide a

10   synchronization correction circuit for correcting divergence
in synchronization between a master and a slave.

For this purpose, the synchronization correction circuit
according to the present invention comprises: a
synchronization signal generating section and an interface

15   control section. The synchronization signal generating
section successively receives packets generated in accordance
with a designated cycle, from an external source, and
generates a packet synchronization signal in synchronization
with the reception cycle of these packets. The interface

20   control section generates a transfer clock for each
respective data element contained in the packets, on the
basis of an internal clock. Additionally, the interface
control section makes the cycle of the transfer clock
corresponding to the last data element of the packet longer

25   than the transfer clocks corresponding to the other data
elements, if the actual cycle of the packet synchronization
signal is longer than the designated cycle, and makes the

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cycle of the transfer clock corresponding to the last data element of the packet shorter than the transfer clocks corresponding to the other data elements, if the actual cycle of the packet synchronization signal is shorter than the designated cycle.

With such composition, it is possible to correct the cycle of the transfer clock in such a manner that it is synchronized with the packet reception cycle.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the present invention will be better understood from the following description taken in connection with the accompanying drawings, in which:

Fig. 1 is a block diagram showing the composition of a synchronization correction circuit according to a first embodiment of the present invention;

Fig. 2 is a circuit diagram showing the internal structure of the interface control section shown in Fig. 1;

Fig. 3 is a timing chart illustrating the operation of a synchronization correction circuit according to a first embodiment of the present invention;

Fig. 4 is a timing chart illustrating the operation of a synchronization correction circuit according to a first embodiment of the present invention;

Fig. 5 is a timing chart illustrating the operation of a synchronization correction circuit according to a first embodiment of the present invention;

Fig. 6 is a block diagram showing the composition of a synchronization correction circuit according to a second embodiment of the present invention;

Fig. 7 is a circuit diagram showing the internal

5 structure of the interface control section shown in Fig. 6;

Fig. 8 is a block diagram showing the composition of a synchronization correction circuit according to a third embodiment of the present invention;

Fig. 9 is a circuit diagram showing the internal

10 structure of the interface control section shown in Fig. 8;

Fig. 10 is a block diagram showing the composition of a synchronization correction circuit according to a fourth embodiment of the present invention;

Fig. 11 is a circuit diagram showing the internal

15 structure of the interface control section shown in Fig. 10;

Fig. 12 is a block diagram showing the composition of a synchronization correction circuit according to a fifth embodiment of the present invention;

Fig. 13 is a circuit diagram showing the internal

20 structure of the interface control section shown in Fig. 12;

Fig. 14 is a conceptual diagram illustrating a packet structure for audio data;

Figs. 15(A), 15(B) and 15(C) are conceptual diagrams for explaining an audio data communication method, respectively;

25 Fig. 16 is a block diagram showing the internal structure of a conventional audio data processing circuit;

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Fig. 17 is a timing chart showing the operation of a conventional audio data processing circuit; and

Fig. 18 is a timing chart showing the operation of a conventional audio data processing circuit.

5   DESCRIPTION OF THE PREFERRED EMBODIMENTS

With reference to the drawings, embodiments of a synchronization correction circuit according to the present invention will be hereinafter be described. It should be noted that these drawings show an outline of size, shape and

10   positional arrangement of the respective constituent parts only to an extent necessary for appreciating the present invention, and consequently, the present invention is not limited to the examples shown in the drawings. Also, the numerical values in the following explanation are merely

15   examples, and not intended to limit the present invention in any way.

First Embodiment

Below, a synchronization correction circuit according to a first embodiment of the present invention will be described

20   with reference to Fig. 1 to Fig. 5, taking an example where the synchronization correction circuit is employed in a Bluetooth audio data processing circuit.

Fig. 1 is a block diagram showing the composition of an audio data processing circuit according to this embodiment.

25   As shown in Fig. 1, the audio data processing circuit 100 comprises: a baseband processing section 110, an audio data

converting section 120, an interface control section 130, a CPU bus 140, and a CPU 150.

Each time that a sync word of a received packet (see Fig. 14) is detected, the baseband processing section 110 extracts the payload section from that received packet and sends it to the audio data converting section 120. Furthermore, the baseband processing section 110 generates a transmission packet by using the audio data received from the audio data converting section 120. The baseband processing section 110 is also provided with a synchronization signal generating section 111. The synchronization signal generating section 111 generates a packet synchronization signal PSYNC which is synchronized with the cycle at which the sync words of the received packets are detected.

Upon receiving a packet, the audio data converting section 120 converts the audio data received from the baseband processing section 110, as necessary, and transfers it to the interface control section 130. Moreover, upon transmitting a packet, the audio data converting section 120 reconverts the audio data received from the interface control section 130, as necessary, and transfers it to the baseband processing section 110. The data formats which can be converted and reconverted by the audio data converting section 120 are, for example, the same as those used in a conventional audio data processing circuit.

The interface control section 130 then generates a transfer clock PCMCLK and a transfer synchronization signal

PCMSYNC, by using the packet synchronization signal PSYNC input from the synchronization signal generating section 111. The transfer clock PCMCLK and the transfer synchronization signal PCMSYNC are transmitted to a PCM codec interface

5   circuit (not illustrated). Furthermore, the interface control section 130 sends and receives audio data (PCM data), to and from the PCM codec interface circuit. The PCM codec interface circuit uses the transfer clock PCMCLK and the transfer synchronization signal PCMSYNC for both transmitting and

10   receiving packets.

The synchronization correction circuit according to this embodiment comprises the synchronization signal generating section 111 and the interface control section 130.

Fig. 2 is a block diagram showing the constituent

15   elements of an interface control section 130. The interface control section 130 shown in Fig. 2 comprises a transmission interval counter 201, three comparators 202, 203, 204, a type selector 205, a transfer clock generating section 206, and a transfer synchronization signal generating section 207.

20   The transmission interval counter 201 counts the clock number of a measurement clock MCLK, and outputs the count value CNT. The transmission interval counter 201 halts the count when a detection signal Sd has a High level, and it resets the count value when the packet synchronization signal

25   PSYNC is input. In this embodiment, the measurement clock has a frequency of 1 MHz.

Comparator 202 inputs the count value CNT to one input

terminal, and inputs the numerical value "1250"

(corresponding to the packet interval for type I, in other

words, 1250 μs) to the other input terminal. If the two

5   inputs are not matching, it outputs a low-level signal, and

if the two inputs are matching, then it outputs a high-level

signal. Similarly, the comparator 203 inputs a count value

CNT via one input terminal and inputs the numerical value

"2500" (corresponding to the packet interval for type II) via

10   the other input terminal; and it outputs a high-level signal

only when the two input values are matching. The comparator

204 inputs the count value CNT via one input terminal and

inputs a numerical value "3750" (corresponding to the packet

interval for type III) via the other input terminal; and it

15   outputs a high-level signal only when the two input values

are matching.

The type selector 205 selects the output signal from one

of comparator 202, 203 or 204. The comparator selected by the

type selector 205 is determined by control implemented by the

20   CPU 150, or the like, in accordance with the type of packet

(type I, II or III) used in communication. The type of packet

used in communication is conveyed from the master to the

slave, and input to the CPU 150, for example.

The transfer clock generating section 206 generates a

25   transfer clock PCMCLK in synchronization with the input

timing of the packet synchronization signal PSYNC, and

outputs the transfer clock PCMCLK to a latter-stage PCM codec

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interface circuit (not illustrated). If, for example, one packet consists of 8 bits × 10 words, then a transfer clock PCMCLK having a cycle of 1/80 of the packet synchronization signal PSYNC is generated. When the next packet

5   synchronization signal PSYNC is input, the transfer clock generating section 206 resets the clock generation function and starts to generate a transfer clock PCMCLK that is synchronized with the new packet synchronization signal PSYNC. Furthermore, if the type selector 205 output is high-level,

10   then the transfer clock generating section 206 fixes the transfer clock PCMCLK to low-level.

The transfer synchronization signal generating section 207 generates a transfer synchronization signal PCMSYNC from the transfer clock PCMCLK, and then outputs it to the latter-

15   stage PCM codec interface circuit. For example, if one word consists of 8 bits, then the transfer synchronization signal generating section 207 will generate and output one transfer synchronization signal PCMSYNC, each time that 8 transfer clocks PCMCLK have been input.

20   Next, the operation of the synchronization correction circuit according to this embodiment will be described with reference to Fig. 3 to Fig. 5.

When operating as a master device, the audio data processing circuit 100 does not use the synchronization

25   correction circuit 111, 130 according to this embodiment. In other words, in an audio data processing circuit 100 operating as a master device, the synchronization signal

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generating section 111 does not generate a packet synchronization signal PSYNC. The transfer clock PCMCLK and the transfer synchronization signal PCMSYNC are generated in a similar manner to the prior art.

5   On the other hand, if the audio data processing circuit 100 is operating as a slave device, then a transfer clock PCMCLK and a transfer synchronization signal PCMSYNC are generated by means of the synchronization correction circuit 111, 130. This is described below with reference to an

10   example where the packet transmission and reception interval is 1250 μs.

        Fig. 3 is a timing chart illustrating the operation of an interface control section 130 in a case where the master and slave have matching operating frequencies.

15   The transmission interval counter 201 is reset at the rise timing of the packet synchronization signal PSYNC and starts a new count of the measurement clock MCLK. The count value CNT is sent successively to the comparators 202, 203 and 204.

20   As described above, comparators 202, 203 and 204 compare these count values CNT with a set value of 1250, 2500 or 3750. If the count value CNT has not yet reached the set value, then the output of the respective comparators 202, 203, 204 is set to low-level.

25   The type selector 205 selects the output of comparator 202 and transmits this output to the transfer clock generating section 206.

This transfer clock generating section 206 generates and outputs a transfer clock PCMCLK of a prescribed cycle, when the input from the type selector 205 is low-level.

Also, in this case, the transfer synchronization signal generating section 207 outputs a transfer synchronization signal PCMSYNC, each time the clock number of the transfer clock PCMCLK reaches the number of bits in one word.

In the example in Fig. 3, the operating frequencies of the master and slave are matching, and therefore, when the count value CNT of the transmission interval counter 201 has reached "1249" (in other words, the clock number of the measurement clock MCLK has reached 1250), the next packet synchronization signal PSYNC is input to the transmission interval counter 201. Thereby, the count value CNT of the transmission interval counter 201 is reset. The transmission interval counter 201 restarts a count from "0".

Thereafter, the interface control section 130 repeats the generation and output of the transfer clock PCMCLK and the transfer synchronization signal PCMSYNC, in a similar manner.

Fig. 4 is a timing chart illustrating the operation of an interface control section 130 in a case where the operating frequency of the slave is higher than the operating frequency of the master.

The operation immediately after the start of the count is the same as that illustrated in Fig. 3. In other words, the transmission interval counter 201 successively outputs

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the count value CNT of the measurement clock MCLK, the

comparators 202, 203, 204 compare the count value CNT with

the set value, and the type selector 205 selects the outputs

of the comparator 202 and transmits this output to the

5   transfer clock generating section 206. The transfer clock

generating section 206 generates and outputs a transfer clock

PCMCLK having a prescribed cycle, whilst the input from the

type selector 205 is at low-level.

Here, whereas the measurement clock MCLK is synchronized

10   to the system clock in the slave, the packet synchronization

signal PSYNC is synchronized to the system block in the

master. Therefore, if the operating frequency of the slave is

higher than the operating frequency of the master, the count

value CNT of the transmission interval counter 201 will reach

15   "1250" before the next packet synchronization signal PSYNC is

input. Thereby, the output of the comparator 202 will change

to high-level, and hence the output Sd of the type selector

205 will also change to high-level. When the signal Sd

changes to high-level in this manner, the transmission

20   interval counter 201 halts the count. Thereby, the count

value CNT remained unchanging at "1250". Furthermore, when

the signal Sd assumes a high-level, the transfer clock

generating section 206 fixes the transfer clock PCMCLK to a

low-level.

25   Thereupon, when the next packet synchronization signal

PSYNC is input, the count value of the transmission interval

counter 201 is reset and the count value CNT becomes "0",

whereby the signal Sd assumes a low level. Consequently, the transmission clock generating section 206 restarts generation of the transfer clock PCMCLK, in accordance with the input timing of the packet synchronization signal PSYNC.

5   In this way, if the operating frequency of the slave is greater than the operating frequency of the master, then the period of the transfer clock PCMCLK is corrected by lengthening the low-level period of the transfer clock PCMCLK corresponding to the final data element of the word. The

10   transfer synchronization signal generating section 207 uses this transfer clock PCMCLK to generate a transfer synchronization signal PCMSYNC.

Thereafter, the interface control section 130 similarly repeats the operations of generating and outputting transfer

15   clock PCMCLK and the transfer synchronization signal PCMSYNC.

Fig. 5 is a timing chart illustrating the operation of the interface control section 130 in a case where the operating frequency of the slave device is lower than the operating frequency of the master device.

20   The operation immediately after the start of counting is similar to that illustrated in Fig. 3.

If the operating frequency of the slave is lower than the operating frequency of the master, then the subsequent packet synchronization signal PSYNC will be input before the

25   count value CNT of the transmission interval counter 201 reaches "1249" (in other words, before 1250 μs has passed since the input of the packet synchronization signal PSYNC).

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In this case, in the transfer clock generating section 206, the transfer clock PCMCLK will be raised to high-level, at the input timing of the new packet synchronization signal PSYNC.

5   If the operating frequency of the slave is lower than the operating frequency of the master in this way, then the cycle of the transfer clock PCMCLK is corrected by shortening the low-level period of the transfer clock PCMCLK corresponding to the last data element of the word.

10   Thereafter, the transfer synchronization signal generating section 207 uses this transfer clock PCMCLK to generate a transfer synchronization signal PCMSYNC.

Thereupon, the interface control section 130 repeats the generation and output of the transfer clock PCMCLK and

15   transfer synchronization signal PCMSYNC, in a similar manner.

As described previously, according to the synchronization correction circuit relating to this embodiment, the period of the transfer clock PCMCLK and the transfer synchronization signal can be corrected in such a

20   manner that they are synchronized with the cycle of the packet synchronization signal PSYNC, in other words, the reception cycle for packets from the master. Therefore, according to this embodiment, it is possible to improve the quality of audio data communicated by a Bluetooth system.

Second Embodiment

Next, a synchronization correction circuit according a
second embodiment of the present invention will hereinafter
be described with reference to Fig. 6 and Fig. 7.

5   Fig. 6 is a block diagram showing the composition of an
audio data processing circuit according to this embodiment.
In this diagram, the constituent elements labelled with the
same numerals as Fig. 1 indicate elements which are the same
as those shown in Fig. 1. In the audio data processing

10   circuit 600 according to this embodiment, the composition of
the synchronization signal generating section 601 provided
inside the baseband processing section 110, and the
composition of the interface control section 610 are
different to the audio data processing circuit 100 according

15   to the first embodiment.

Similarly to the first embodiment, the synchronization
signal generating section 601 generates a packet
synchronization signal PSYNC using the cycle at which
received packet sync words are detected. However, in this

20   embodiment, rather than generating a packet synchronization
signal PSYNC by synchronizing with the reception cycle for
one packet, a packet synchronization signal PSYNC is
generated every 7500 μs. Here, 7500 μs is the smallest common
multiple of 1250 μs, 2500 μs and 3750 μs, which are the

25   transmission intervals of packet transmission types I, II and
III. In other words, in this embodiment, if the communicated
packets are type I (packet transmission cycle of 1250 μs),

then a packet synchronization signal PSYNC is generated in

synchronization with the each reception cycle of 6 packets;

if the communicated packets are type II (packet transmission

cycle of 2500 μs), then a packet synchronization signal PSYNC

5   is generated in synchronization with each reception cycle of

3 packets; and if the communicated packets are type III

(packet transmission cycle of 3750 μs), then a packet

synchronization signal PSYNC is generated in synchronization

with each reception cycle of 2 packets.

10   Similarly to the interface control section 130 according

to the first embodiment, the interface control section 610

uses the packet synchronization signal PSYNC to generate a

transfer clock PCMCLK and a transfer synchronization signal

PCMSYNC, which are transferred to the latter-stage PCM codec

15   interface circuit (not illustrated). As described hereinafter,

the interface control section 610 according to this

embodiment differs from the interface control section 130

according to the first embodiment in that it comprises only

one comparator.

20   The synchronization correction circuit according to the

present embodiment comprises the synchronization signal

generating section 601 and the interface control section 610.

     Fig. 7 is a block diagram showing the constituent

elements of the interface control section 610. The interface

25   control section 610 in Fig. 7 comprises a transmission

interval counter 701, comparator 702, transfer clock

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generating section 703 and transfer synchronization signal generating section 704.

Similarly to the transmission interval counter 201 according to the first embodiment, the transmission interval counter 701 counts the clock number of the measurement clock MCLK (for example, 1 MHz) and outputs a count value CNT, whilst the detection signal Sd is low-level. Moreover, the transmission interval counter 701 halts the count if the detection signal Sd is high-level, and it resets the count value if the packet synchronization signal PSYNC is input.

The comparator 702 inputs the count value CNT via one input terminal and inputs the numerical value "7500" via the other input terminal. Thereupon, if the two input values are not matching, then a low-level signal is output, and if the two input values are matching, then it outputs a high-level signal.

Similarly to the transfer clock generating section 206 according to the first embodiment, the transfer clock generating section 703 generates a transfer clock PCMCLK in synchronization with the input timing of the packet synchronization signal PSYNC, and when the next packet synchronization signal PSYNC is input, it reset the clock generation operation and starts generation of a transfer clock PCMCLK that is synchronized with the new packet synchronization signal PSYNC, and furthermore, if the signal Sd is high-level, then it fixes the transfer clock PCMCLK to low-level.

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Similarly to the transfer synchronization signal
generating section 207 according to the first embodiment, the
transfer synchronization signal generating section 704
generates and outputs a transfer synchronization signal

5   PCMSYNC from the transfer clock PCMCLK.

As described above, by means of the synchronization
correction circuit 601, 610 according to this embodiment, the
clock width of the transfer clock PCMCLK is corrected every
7500 μs. In other words, if the communicated packets are type

10   I, then synchronization correction is carried out at a ratio
of once for every 6 packets' equivalent of the transfer clock
PCMCLK. Moreover, if the communicated packets are type II,
then synchronization correction is carried out at a ratio of
once for every three packets' equivalent of the transfer

15   clock PCMCLK. Similarly, if the communicated packets are type
III, then synchronization correction is carried out at a
ratio of once for every two packets' equivalent of the
transfer clock PCMCLK. If the divergence in synchronization
between the master and slave devices is very small, then even

20   if synchronization correction is carried out at cycles of the
above order, it is still possible to obtain synchronization
of sufficiently high accuracy.

As described above, according to the synchronization
correction circuit relating to this embodiment, it is

25   possible to correct the cycle transfer clock PCMCLK and the
transfer synchronization signal PCMSYNC in such a manner that
they are synchronized with the cycle of the packet

synchronization signal PSYNC, in other words, the reception

cycle of packets from the master device. Consequently,

according to this embodiment, it is possible to improve the

quality of audio data communicated by a Bluetooth system.

5   Moreover, since the synchronization correction circuit

according to this embodiment has one comparator and does not

require a type selector, the scale of the circuitry is

smaller than the synchronization correction circuit according

to the first embodiment, and hence power consumption is lower.

10   Third embodiment

Next, a synchronization correction circuit according to

a third embodiment of the present invention will hereinafter

be described with reference to Fig. 8 and Fig. 9.

Fig. 8 is a block diagram showing the composition of an

15   audio data processing circuit according to this embodiment.

In Fig. 8, the constituent elements labelled with the same

numerals as Fig. 1 indicate the same elements as those shown

in Fig. 1. In the audio data processing circuit 800 according

to this embodiment, the composition of the interface control

20   section 810 differs from that of the audio data processing

circuit 100 according to the first embodiment.

The interface control section 810 uses the packet

synchronization signal PSYNC to generate a transfer clock

PCMCLK and a transfer synchronization signal PCMSYNC. The

25   interface control section 810 according to this embodiment

inputs a comparison value C and a number of stages F from the

CPU 150. Here, the comparison value C is the packet

transmission interval designated by the master device, and in the case of type I, this is "1250", in the case of type II, it is "2500", and in the case of type III, it is "3750". The number of stages F is a value indicating the frequency at

5 which synchronization correction is implemented. In other words, the interface control section 810 according to this embodiment performs synchronization correction each time F packet synchronization signals PSYNC are input.

The synchronization correction circuit according to this

10 embodiment comprises the synchronization signal generating section 111 and the interface control section 810.

Fig. 9 is a block diagram showing the principal composition of the interface control section 810. The interface control section 810 shown in Fig. 9 comprises a

15 transmission interval counter 901, a comparison value register 902, a transmission interval comparator 903, a comparison stage number counter 904, a stage number register 905, a stage number comparator 906, a transfer clock generating section 907, and a transfer synchronization signal

20 generating section 908.

The transmission interval counter 901 counts the clock number of the measurement clock MCLK (for example, 1 MHz) and outputs a count value CNT; when the detection signal Sd is high-level, it halts the count, and when the packet

25 synchronization signal PSYNC is input, it resets the count value.

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The comparison value register 902 holds a comparison value C input from the CPU 150.

The comparator 903 inputs a count value CNT via one input terminal, and inputs the stored value in the comparison value register (in other words, comparison value C) to the other. If the two input values are not matching, it outputs a low-level signal, and if the tow input values are matching, then it outputs a high-level signal.

The comparison stage number counter 904 counts the number of times that the output of the comparator 903 has risen from low-level to high-level, in other words, the number of times that the count value CNT has reached the comparison value C.

The stage number register 905 holds a number of stages F input from the CPU 150.

The stage number comparator 906 inputs the output value of the comparison stage number counter 904 and the stored value in the stage number counter 904, in other words, the number of stages F. If the two input values are not matching, then it outputs a low-level signal, and if the two input values are matching, then it outputs a high-level signal. The output value of the stage number comparator 906 is transmitted as a detection signal Sd to the transfer clock generating section 907 and the transmission interval counter 901.

Similarly to the transfer clock generating section 206 according to the first embodiment, the transfer clock

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generating section 907 generates a transfer clock PCMCLK in
synchronization with the input timing of the packet
synchronization signal PSYNC, and when the next packet
synchronization signal PSYNC is input, it resets the clock
5   generation function and starts generation of a transfer clock
PCMCLK which is synchronized with the new packet
synchronization signal PSYNC, in addition to which, it fixes
the transfer clock PCMCLK to low-level when the signal Sd is
high-level.

10   Similarly to the transfer synchronization signal
generating section 207 according to the first embodiment, the
transfer synchronization signal generating section 908
generates a transfer synchronization signal PCMSYNC from the
transfer clock PCMCLK and outputs same to the PCM codec
15   interface circuit.

Next, the operation of the synchronization correction
circuit according to this embodiment will be described.

Firstly, a comparison value C and stage number F are
input from the CPU 150 as initial settings of the audio data
20   processing circuit 800, and are stored in the registers 902,
905.

Thereupon, the transmission interval counter 901 starts
a count. The transmission interval counter 901 is reset at
the rise timing of the packet synchronization signal PSYNC,
25   and starts a new count of the measurement clock MCLK. The
count value CNT is transmitted to the transmission interval
comparator 903.

The transmission interval comparator 903 compares the count value CNT with the comparison value C. If the count value CNT has not reached the comparison value, then the output of the comparator 903 is low-level.

5   When the count value CNT reaches the comparison value C, the output of the comparator changes to high-level, and the count value of the comparison stage number counter 904 is incremented by '1'. The stage number comparator 906 compares the count value of the comparison stage number counter 904

10   with the stage number F. If the count value has reached the stage number F, then the stage number comparator 906 sets the signal Sd to high-level.

Similarly to the first embodiment, the transmission interval counter 901 halts the count operation whilst the

15   signal Sd is at high-level. The transmission interval counter 901 resets the count value CNT, when the next packet synchronization signal PSYNC is input. Moreover, in this case, the comparison stage number counter 904 is also reset.

Similarly to the first embodiment, if the operating

20   frequency of the slave is higher than the operating frequency of the master, then the output of the comparator 903 will change to high-level, before the next packet synchronization signal PSYNC is input. Therefore, in this case, the output signal Sd of the stage number comparator 906 assumes a high-

25   level at each F input cycles of the packet synchronization signal PSYNC. The transfer clock generating section 907

corrects the low-level period of the transfer clock PCMCLK, each time that the signal Sd becomes high-level.

On the other hand, if the operating frequency of the slave is lower than the operating frequency of the master, then the signal Sd will never assume high-level. In this case, similarly to the first embodiment, the transfer clock generating section 907 corrects the clock width of the transfer clock, each time the packet synchronization signal PSYNC is input (in other words, at a rate of once every C µs).

As described above, according to the synchronization correction circuit relating to this embodiment, the cycles of the transfer clock PCMCLK and the transfer synchronization signal PCMSYNC can be corrected in such a manner that they are synchronized with the cycle of the packet synchronization signal PSYNC, in other words, the reception cycle of packets from the master device. Consequently, according to this embodiment, it is possible to improve the quality of audio data communications by a Bluetooth system.

Moreover, since the synchronization correction circuit according to this embodiment comprises two comparators, it has lower power consumption than the synchronization correction circuit according to the first embodiment.

On the other hand, the frequency with which divergence in synchronization is corrected can be set freely, and therefore, the range of synchronization divergence that can be corrected is greater than that afforded by the

synchronization correction circuit according to the second

embodiment.

Fourth Embodiment

Next, a synchronization correction circuit according to

5   a fourth embodiment of the present invention will hereinafter

be described with reference to Fig. 10 and Fig. 11.

Fig. 10 is a block diagram showing the composition of an

audio data processing circuit according to this embodiment.

In Fig. 10, the constituent elements having the same labels

10   as those of Fig. 8 indicate elements that are the same as

those shown in Fig. 8.

The audio data processing circuit 1000 according to this

embodiment differs from the audio data processing circuit 800

according to the third embodiment in that the interface

15   control section 1010 generates and outputs an interrupt

signal BRK. The interrupt signal BRK is output each time that

correction of the transfer clock PCMCLK is implemented, when

the operating frequency of the slave is higher than the

operating frequency of the master. This interrupt signal BRK

20   is sent via the bus 140 to the CPU 150.

Fig. 11 is a block diagram showing the principal

composition of the interface control section 1010. In Fig. 11,

constituent elements having the same labels as those of Fig.

9 indicate elements which are the same as those shown in Fig.

25   9. In other words, the internal structure of the interface

control section 1010 according to this embodiment is the same

as the interface control section 810 shown in Fig. 9, with

29

the exception that it comprises a structure for outputting the output from the stage number comparator 906 to the bus 140 as an interrupt signal BRK.

According to this composition, the CPU 150 is able to detect that the operating frequency of the slave is higher than the operating frequency of the master, by means of receiving the interrupt signal BRK. If, on the other hand, the interrupt signal BRK is not received, then the CPU 150 can detect that the operating frequency of the slave is either equal to the operating frequency of the master, or lower than the operating frequency of the master. Thereby, the CPU 150 is able to adjust the operating frequency of the system clock, by means of the interrupt signal BRK, for example.

In other words, the synchronization correction circuit according to the present embodiment is able to perform synchronization correction by correcting the cycle of the system clock, in addition to performing synchronization correction similar to that in the third embodiment. Therefore, according to this embodiment, it is possible to correct the cycles of the transfer clock PCMCLK and the transfer synchronization signal PCMSYNC in a more accurate fashion.

Moreover, the operation of other circuits provided in the audio data processing circuit 1000 can also be corrected readily by correction of the system clock.

Fifth Embodiment

A fifth embodiment of the present invention will hereinafter be described below with reference to Fig. 12 and Fig. 13.

5   Fig. 12 is a block diagram showing the composition of an audio data processing circuit according to this embodiment. In Fig. 12, the constituent elements having the same labels as those of Fig. 10 indicate elements which are the same as those shown in Fig. 10.

10   Similarly to the fourth embodiment, the CPU 1210 successively inputs interrupt signals BRK from the interface control section 1220, and derives and outputs the average value ARG for the interval at which packets are transmitted by the master device, from the first prescribed number of

15   interrupt signals BRK.

The interface control section 1220 internally stores the average value ARG input from the CPU 1210. The interface control section 1220 uses this average value ARG, in place of the comparison value C, in the subsequent synchronization

20   correction process.

Fig. 13 is a block diagram showing the principal composition of the interface control section 1220. In Fig. 13, the constituent elements having the same labels as those of Fig. 11 are elements which are the same as those shown in Fig.

25   11. In other words, the interface control section 1220 according to this embodiment differs from the interface

control section 1010 in Fig. 11 in that it is provided with

an average value storage circuit 1301 and a selector 1302.

The average value storage circuit 1301 stores the

average value ARG input from the CPU 1210.

5   Before the average value ARG has been stored in the

average value storage circuit 1301, the selector 1302 selects

the output of the comparison value register 902 and transfers

the comparison value C to the transmission interval

comparator 903, and after the average value ARG has been

10   stored in the average value storage circuit 1301, the

selector 1302 selects the output of the average value storage

circuit 1301 and transfers the average value ARG to the

transmission interval comparator 903.

As illustrated in Fig. 13, it is also possible for the

15   average value storage circuit 1301 to calculate the average

value ARG by reading in the count value CNT of the

transmission interval counter 901, in a successive fashion.

In this embodiment, firstly, a comparison value C and a

stage number F are input from the CPU 1210 as initial

20   settings of the audio data processing circuit 1200, and are

stored in the registers 902, 905. When the count of the

transmission interval counter 901 is started, the

transmission interval comparator 903 successively compares

the count values CNT and the comparison value C. Similarly to

25   the third and fourth embodiments, the counting operation

performed by the comparison stage number counter 904 and the

comparison operation performed by the stage number comparator

906 are repeated. Moreover, also similarly to the third and fourth embodiments, the transmission clock generating section 907 generates a transfer clock PCMCLK which is corrected for synchronization. The transfer synchronization signal generating section 908 generates a transfer synchronization signal PCMSYNC from this transfer clock PCMCLK.

If the operating frequency of the slave is higher than the operating frequency of the master, then similarly to the third and fourth embodiments, the output signal Sd of the stage number comparator 906 will become high-level, at each F cycles of the packet synchronization signal PSYNC. This signal Sd is input to the CPU 1210 as an interrupt signal BRK.

As described previously, the CPU 1210 derives an average value ARG for the packet transmission interval from a prescribed number of interrupt signals BRK. The CPU 1210 sends this average value ARG to the interface control section 1220.

The interface control section 1220 stores the average value ARG input from the CPU 1210, in the average value storage circuit 1301. In this case, the selection made by the selector 1302 is switched to the average value storage circuit 1301, by control performed by the CPU 1210, or the like.

Thereupon, the transmission interval comparator 903 successively compared the count value CNT and the average value ARG, and if these values, CNT and ARG, are not matching, it outputs a low-level signal, whereas if they are matching,

it outputs a high-level signal. The operation of the comparison stage number counter 904, stage number comparator 906, transfer clock generating section 907 and transfer synchronization signal generating section 908 are the same as their respective operations when using the comparison value C.

As described above, according to the synchronization correction circuit relating to this embodiment, it is possible to correct the cycles of the transfer clock PCMCLK and the transfer synchronization signal PCMSYNC, in such a manner that they are synchronized with the cycle of the packet synchronization signal PSYNC, in other words, the reception cycle of packets from the master. Therefore, according to this embodiment, it is possible to improve the quality of audio data communicated by a Bluetooth system.

Moreover, according to this embodiment, since the comparison value C is used only for an initial prescribed number of times, whereupon an average value ARG is used, it is possible to reduce the frequency at which the stage number comparator 906 outputs the signals Sd, BRK, the frequency at which the transmission interval counter 901 halts the count, and so on, and therefore it is possible to reduce the power consumption of the interface control section 1220.

In the foregoing embodiments, the synchronization correction circuit relating to the present invention was described with reference to an example where it was applied to an audio data processing circuit for a Bluetooth system, but the present invention may also be employed in

synchronization correction circuits for other types of data

processing circuits, provided that these handle communication

packets.